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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. |
|---|---|---|---|
| 09/757,439 | 01/10/01 | BELGARD R | RAB 2001-1 |

TM02/0913

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| EXAMINER | |
|---|---|
| NGUYEN, T | |
| **ART UNIT** | **PAPER NUMBER** |
| 2187 | 4 |

**DATE MAILED:** 09/13/01

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

# Office Action Summary

| Application No. | Applicant(s) |
|---|---|
| 09/757,439 | Belgard |
| **Examiner** | **Group Art Unit** |
| TNguyen | 2187 |

*—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

**Status**

☒ Responsive to communication(s) filed on 4/16/01.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

**Disposition of Claims**

☒ Claim(s) 38-66 is/are pending in the application.

Of the above claim(s)____ is/are withdrawn from consideration.

☒ Claim(s) 38-59, 60-66 is/are allowed.

☒ Claim(s) 57-59 is/are rejected.

☐ Claim(s)____ is/are objected to.

☐ Claim(s)____ are subject to restriction or election requirement.

**Application Papers**

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. § 119 (a)-(d)**

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number)____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received:____.

**Attachment(s)**

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 3

☐ Interview Summary, PTO-413

☒ Notice of Reference(s) Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other____

**Office Action Summary**

## DETAILED ACTION

1. Claims 38-66 are pending.

2. The IDS, filed 4/16/01, has been considered.

### *Double Patenting*

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

**A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).**

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 57-59 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 36 of U.S. Patent No. 6,226,733. Although the conflicting claims are not identical, they are not patentably distinct from each other because the patent claim 36 contain all of the limitations of claims 57-58, and more limitations (steps d & e of claim 36 in patent). Although the patent's claim has more limitations than the current application's claim, it would have been obvious to one of ordinary skills in the art to remove limitations from the claim if the effects of the limitation is not desired. As to claim 59, the speculative memory reference of claim 36 in the patent is toward a memory, which is a cache (See patent's specification).

***Allowable Subject Matter***

5. Claims 38-56,60-66 are allowed for the reasons below.

6. As to claim 38, the prior art of record does not teach a system for performing address translation in a processor employing both segmentation and optional independent paging having a page cache that provides an actual physical page frame address and accessed by using a page field of a fully calculated linear address, and a speculative physical page frame address generator for generating a speculative physical address before the actual physical address is generated by combining the offset portions to the page frames..

7. Claims 39-43 are also allowable for incorporating the limitations of claim 38, and further limitations.

8. As to claim 44, the prior art of record does not teach nor suggest the claimed circuit for performing memory accesses in a system that uses virtual address having both a segment identifier and a segment offset to generate a linear address, generating an caching a calculated physical address based on the linear address, generating a tentative physical address, wherein the tentative physical address is used for memory access unless it is different from the calculated physical address.

9. Claims 45-51 are also allowed for incorporating the limitations of claim 44, and further limitations.

10. As to claim 52, the prior art of record does not teach nor suggest a computer system using segmentation and optional independent paging for address translations comprising: a fast physical address circuit generating a fast physical address comprised of a stored page frame with a page offset portion derived from a virtual address; wherein the fast physical address is generated prior to the generation of the calculated physical address.

11. Claims 53-56 are also allowed for incorporating the limitations of claim 52, and further limitations.

12. As to claim 60, the prior art of record does not teach nor suggest a method of performing memory references in a processor that employs both segmentation and optional independent paging during an address translation comprising: performing an actual address translation from a virtual address by calculating a linear address based on both a segmentation identifier and an offset associated with the virtual address, generating an actual physical address based on the calculated linear address, and perform a speculative address translation from the virtual address using portions of the linear address and actual address information from a prior virtual address translation to produce a speculative physical address.

13. Claims 61-62 are also allowed for incorporating the limitations of claim 60, and further limitations.

14. As to claim 63, the prior arts of record does not teach the claimed method of performing memory accesses in a microprocessor system using a virtual address having a segment identifier and a segment offset with the following steps: using a second cache containing physical address

information to generate a tentative physical address in parallel with the generating a calculated linear address and before the step of generating a calculated physical address using a physical address information in a first cache to generate a calculated physical address; completing the tentative memory access to the cache when the tentative physical address and calculated physical address are the same while aborting the tentative memory access and perform a second memory access based on the calculated physical address when the tentative and calculated physical addresses are different.

15. Claims 64-66 are also allowed for incorporating the limitations of claim 63, and further limitations.

***Conclusion***

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Than Nguyen whose telephone number is (703) 305-3866.

17. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9700.

Than Nguyen

August 31, 2001